G O D W I N G R U B E R

Attorneys
A Professional Corporation

1201 Elm, Suite 1700
Dallas, Texas 75270-2084
214.939.4400
214.760.7332 Fax
godwingruber.com

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To	Company	Phone	Fax
Examiner John Dill	USPTO		1-703-746-6606

From Gary C. Honeycutt (214) 939-8651

Client/Matter Number 50000.2166

Comments

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If you do not receive all materials being transmitted, please call Emily Chantry at (214) 939-8658

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a schematic top view of the partially assembled interconnector according to the first System and Flow of the invention.

FIG. 1B is a schematic cross section of the partially assembled interconnector according to the first System and Flow of the invention.

FIG. 1C is a schematic bottom view of the partially assembled interconnector according to the first System and Flow of the invention.

FIG. 1D is a schematic cross section of the partially assembled interconnector in the process of folding, according to the first System and Flow of the invention.

FIG. 1E is a schematic cross section of a plurality of fine-pitch chip-scale packages prepared for attachment onto the folded interconnector of FIG. 1D.

FIG. 1F is a schematic cross section of a plurality of integrated circuit chips prepared for attachment onto the folded interconnector of FIG. 1D.

FIG. 1G is a schematic cross section of the fully assembled vertical device stack including the fine-pitch chip-scale packages of FIG. 1E.

FIG. 1H is a schematic cross section of the fully assembled vertical device stack including the integrated circuit chips of FIG. 1F, with optional underfilling and/or encapsulation.

FIG. 2A is a schematic top view of the partially assembled interconnector according to the second System and Flow of the invention.

FIG. 2B is a schematic cross section of the partially assembled interconnector according to the second System and Flow of the invention.

FIG. 2C is a schematic bottom view of the partially assembled interconnector according to the second System and Flow of the invention.

FIG. 2D is a schematic cross section of the partially assembled interconnector in the process of folding, according to the second System and Flow of the invention.

FIG. 2E is a schematic cross section of the fully assembled vertical device stack including two packages and passive components.

FIG. 2F is a schematic cross section of the fully assembled vertical device stack including a third package, which has bee fabricated and tested separately.

FIG. 2G is a schematic cross section of the fully assembled vertical stack including three packages and passive components.

FIG. 2H is a schematic cross section of the fully assembled vertical stack including three packages assembled on opposite surfaces of the interconnector.

FIG. 2I is a schematic cross section of the fully assembled vertical stack illustrating an additional example of assembly options provided by the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is related to U.S. Patent # 6,084,778, issued on Jul. 4, 2000 (Malhi, "Three Dimensional Assembly using Flexible Wiring Board"), U.S. Patent Applications # 60/172,186, filed 12/17/1999 (Rolda et al., "Multi-Flip-Chip Semiconductor Assembly"), and # 60/249,385, filed 11/16/2000 (Coyle et al., "Flip-Chip on Film Assembly for Ball Grid Array Packages"), which are herewith incorporated by reference.

Structures and methods according to the invention are described in two examples: the first System and Flow are illustrated in FIGs. 1A through 1H; the second System and Flow are illustrated in FIGs. 2A through 2I.

For the first System & Flow, FIG. 1A shows schematically the top view of a rectangular strip-like interconnector 101. It is made of electrically insulating material which is flexible. A preferred choice is a polyimide film in the thickness range from about 40 to 80 μm; in some instances, it may be thicker. Given enough flexibility, other suitable materials include PCB resin, FR-4 (which is an epoxy resin), or a cyanate ester resin. These materials are commercially available from several sources; in the U.S.A., companies include 3-M and Sheldahl; in Japan, Shinko, Shindo, Sumitomo, and Mitsui; and in Hongkong, Compass. This interconnector has two surfaces; FIG. 1C depicts, in bottom view, the first surface 102, while FIG. 1A depicts, in top view, the second surface 103.

Integral with the interconnector 101 is a plurality of electrically conductive lines 104 (they are depicted, as an example, in the top view of FIG. 1A). These conductive lines 104 are usually patterned from a thin metal foil, preferably between about 15 and 40 μm thick. Suitable

materials include copper, copper alloys, gold, silver, palladium, platinum, and stacked of nickel/gold and nickel/palladium. These conductive lines form on the first surface 102 a first array of electrical entry ports 105 and a second array of exit ports 106. As FIG. 1C shows, these arrays are grouped in separate areas of the interconnector; the entry ports 105 are actually depicted in multiple arrays.

It is important for the present invention that the entry ports 105 are spaced apart by less, center to center, than the exit ports 106 are spaced apart, center to center. While the present invention can be applied to any pitch of the entry or exit ports, preferably, these fine-pitched entry ports 105 are spaced apart from each other by less than 100 μm center to center. In contrast, the relatively wide-pitched exit ports 106 are typically spaced apart considerably more than 100 μm center to center. Since the exit ports 106 provide the attachment sites for the coupling members to other parts, their convenient spacing satisfies a desire often expressed by customers, namely to be provided with solder ball attachment sites convenient for semiconductor board assembly. Frequently, the exit ports 106 provide a common footprint to industry standards for chip-scale packages.

Entry ports 105 are typically made of copper, often with a protective flash of gold. Exits ports 106 have to be solderable and thus have to insure reliable wetting. They may be covered by layers of a refractory metal (such as chromium, molybdenum, titanium, tungsten, or titanium/tungsten alloy) and a noble metal (such as gold, palladium, platinum or platinum-rich alloy, silver or silver alloy).

For some products using the first System & Flow, and for the second System & Flow, the interconnector also has

electrically conductive paths extending through the interconnector from one surface to the opposite surface. The mechanical flexibility of such interconnectors also helps preventing solder ball cracking under mechanical stress due to thermal cycling. As stated above, the interconnector is preferably made of compliant material, such as tape, Kapton™ film, polyimide, or other plastic material, and may contain single or multiple layers of patterned conductors. In this fashion, the flexibility of the base material provides a stress buffer between the thermally mismatched semiconductor chip and the P.C. board, and will relieve some of the strain that develops in the chip solder balls in thermal cycling. Alternatively, an interconnector may be made of epoxies, FR-4, FR-5, or BT resin.

Interconnectors with conductive through-paths are commercially available; for instance Novaclad® and ViaGrid® from Sheldahl, Inc., Northfield, MN. They are typically fabricated by laminating alternative films of electrically insulating and electrically conducting materials into one coherent layer. Connections through individual insulating films are made by laser drilling and metal refilling or plating, and patterning of the conductive films is achieved by ablation or etching. There are numerous designs and variations of interconnectors available.

In the schematic cross section of FIG. 1B, the exit ports on the first surface 102 of the interconnector are depicted as having solder balls 107 attached as coupling members for attachment to other (outside) parts. These solder balls are selected from a group consisting of pure tin, tin alloys including tin/copper, tin/indium, tin/silver, tin/ bismuth, tin/lead, and conductive adhesive compounds.

As used herein, the term solder "ball" does not imply that the solder contacts are necessarily spherical; they may have various forms, such as semispherical, half-dome, truncated cone, or generally bump, or a cylinder with straight, concave or convex outlines. The exact shape is a function of the deposition technique (such as evaporation, plating, or prefabricated units) and reflow technique (such as infrared or radiant heat), and the material composition. Several methods are available to achieve consistency of geometrical shape by controlling amount of material and uniformity of reflow temperature. Typically, the diameter of the solder balls ranges from 0.1 to 0.5 mm, but can be significantly larger.

Further shown in the top view of FIG. 1A are encapsulated devices 108; they are depicted in cross section in FIG. 1B. Examples for such devices are MicroStar ™ Ball Grid Arrays (BGAs) and MicroStarJunior™ packages fabricated by Texas Instruments Incorporated, Dallas, Texas, U.S.A. These devices comprise integrated circuit (IC) chips attached to the interconnector film, wire bonding and transfer molded packages.

The electrically conductive lines 104 indicated in FIG. 1A may contain at least one passive electrical component (not shown in FIG. 1A) integrated into the conductive lines. Examples include resistors, capacitors, inductors, distributed components, and networks of passive components and interconnected structures. Fabrication methods for these integrated components have recently been described in U.S. Patent Application # 60/244,673, filed on 10/31/2000 (Pritchett et al., "Plastic Chip-Scale Package having Integrated Passive Components"), which is herewith incorporated by reference.

As indicated in FIG. 1D, the flexible interconnector strip 101 is folded at the region 120 of the integrated conductive lines between the adjacent areas of the entry ports and exit ports. The folding is such that the entry ports face in one direction while the exit ports face in the opposite direction. As a consequence of this folding, the package bodies 108 touch each other, resulting in a vertically stacked assembly having approximately the outline of a chip-scale package. If desired, they package bodies can be glued together in order to render the tight stacking permanent.

FIGs. 1E and 1F illustrate how the entry ports can be populated with semiconductor devices. FIG. 1E depicts, in schematic cross section, multiple chip-scale devices 130, packaged in an encapsulation 131 and having a plurality of fine-pitch electrical coupling members 132. These coupling members may consist of solder "balls" made of pure tin, a tin alloy as listed above, or a conductive adhesive compound. The pattern of the coupling members 132 is mirror-imaging the pattern of the interconnector entry ports.

As indicated in FIG. 1G, the fine-pitch coupling members 132 of chip-scale devices 130 are attached by surface mounting to the entry ports of the interconnector 101. The result is an assembly of chip-scale packages, generally designated 140, stacked vertically and having a plurality of coupling members 107 suitable for attachment to other, outside parts.

Alternatively, FIG. 1F depicts, in schematic cross section, multiple un-encapsulated IC chips 133, prepared for flip-chip assembly by having a plurality of fine-pitch electrical coupling members 134. These coupling members may consist either of solder "balls" (made of pure tin, tin

alloys as listed above, or a conductive adhesive compound) or of metal bumps selected from a group consisting of gold, copper, copper alloy, or layered copper/nickel/palladium. Another option is z-axis conductive epoxy. The bumps have various shapes, for example rectangular, square, round, or half-dome. For metal bumps, the method of attaching the coupling members 134 to the entry ports of the interconnector is a thermo-compression bonding technique based on metal interdiffusion, as has been practiced previously in the tape-automated-bonding (TAB) fabrication method. The preferred technique for the present invention is a gang-bonding technique for array assembly. This technique has the advantage of fast and low-cost operation while resulting in high quality, reliable attachments. The automated apparatus is commercially available from Shinkawa Corporation, Japan.

FIG. 1H shows as the result an assembly, generally designated 141, of flipped chips 133 and encapsulated devices 108, stacked vertically; the assembly further has a plurality of coupling members 107 suitable for attachment to other, outside parts.

FIG. 1G shows that the packages 131 of devices 130 are spaced apart from the interconnector 101 by gaps 142. The solder balls 132 extend across the gaps, connecting to the interconnector. It is an advantage of this invention to choose the materials so that the significant difference in the coefficient of thermal expansion (CTE) between the semiconductor material of the IC chips and the material typically used for the interconnector can be minimized. It is, therefore, usually not necessary in the assembly of FIG. 1G to strengthen the solder joints (without affecting the electrical connection) by filling the gap 142 with a polymeric material which encapsulates the bumps and fills

any space in the gap between the package and the interconnector ("underfilling" method).

This method of underfilling may, however, be appropriate for the assembly depicted in FIG. 1H. This underfilling material, together with some encapsulating material, is indicated by the schematic outline 142 in FIG. 1H. The encapsulant is typically applied after completion of the assembly. A polymeric precursor, sometimes referred to as the "underfill", is dispensed onto the substrate adjacent to the chip and is pulled into the gap by capillary forces. Typically, the polymeric precursor comprises an epoxy-based material filled with silica and anhydrides. The precursor is then heated, polymerized and "cured" to form the encapsulant. The underfilling method preferred by this invention has been described in U.S. Patent Application # 60/084,440, filed on 05/06/98 (Thomas, "Low Stress Method and Apparatus of Underfilling Flip-Chip Electronic Devices").

For the second System & Flow, FIG. 2A shows schematically the top view of a rectangular strip-like interconnector 201, FIG. 2B its cross section, and FIG. 2C the bottom view. The descriptions for materials, processes, conductive lines 204, exit ports 206, optional integrated passive electrical components, solder balls 207, and packaged devices 208 are analogous to the descriptions in FIGs. 1A, 1B, and 1C. The significant difference is depicted in FIGs. 2B and 2C by the discreet passive components 210 attached to the first surface 202 of the interconnector 201. Consequently, the pattern of the entry ports in FIG. 2C is significantly simplified compared to the pattern in FIG. 1C. It is not specifically highlighted in FIG. 2C; it is implicit in the customized attachment the passive components 210.

Similarly, the folding of flexible interconnector strip 201 at the region 220 of the integrated conductive lines between adjacent areas of the entry and exit ports, as illustrated in FIG. 2D, is analogous to the folding of interconnector 101 in FIG. 1D. As a consequence of this folding, the package bodies 208 touch each other, resulting in a vertically stacked assembly having approximately the outline of a chip-scale package. If desired, they package bodies can be glued together in order to render the tight stacking permanent.

The result is illustrated in FIG. 2E. It is an assembly, generally designated 240, of chip-scale packages 208 and discreet passive electrical components 210 stacked vertically and having a plurality of coupling members 207 (usually solder balls) suitable for attachment to other parts. This assembly in FIG. 2E, like the analogous assemblies in FIGs. 4A and 4B, represents an example of the fist embodiment of this invention:

- FIGs. 1G, 1H, and 2E: A first embodiment of the invention combines two single or dual-chip packages (up to four chips total) with passive components, or with multiple fine-pitch chip-scale packages, or with multiple bumped and flipped chips.
- FIG. 2F: A second embodiment of the invention combines three single or dual-chip packages (up to six chips total) with a third package, which has been fabricated and tested separately.
- FIG. 2G: A third embodiment of the invention combines three single or dual-chip packages (up to six chips total) with passive components, or with

multiple fine-pitch chip-scale packages, or multiple bumped and flipped chips.

- FIG. 2H: A fourth embodiment of the invention combines three single or dual-chip packages (up to six chips total). The invention further provides for a variety of other different combinations.
- FIG. 2I: The invention further provides for a variety of other different combinations. The product is a vertical stack of approximately chip-scale footprint, composed of a plurality of active and passive electrical components and devices.

While this invention has been described in reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modification and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. As an example, the material of the semiconductor chip may comprise silicon, silicon germanium, gallium arsenide, or any other semiconductor material used in manufacturing. It is therefore intended that the appended claims encompass any such modifications or embodiments.